Journal of Materials Research and Technology 41 (2026) 3825–3833

Contents lists available at ScienceDirect

Journal of Materials Research and Technology

journal homepage: www.elsevier.com/locate/jmrt

Microstructure and thermal performance of lotus-type porous Cu/solder composite joints

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ARTICLE INFO

Keywords:
Thermal resistance
Thermal conductivity
Lotus-type porous Cu
Cu/solder composite
Die-attach

With the miniaturization and improved efficiency of power modules, the increase in heat generation density has become a critical issue. Therefore, it is essential to develop bonding layers with high heat dissipation performance. In this study, the relationship between the structure, equivalent thermal conductivity, and thermal resistance of a previously proposed lotus Cu/solder composite (LSC) joint was investigated to further reduce thermal resistance. Estimations based on the rule of mixtures indicated that reducing the solder thickness, void fraction, and intermetallic compound (IMC) thickness was effective in lowering the thermal resistance. The factors critical in achieving a thinner solder layer and lower void fraction include the use of a vacuum process, an appropriate solder amount, and low bonding pressure. Steady-state thermal measurements revealed that thinner solder layers and lower void fractions significantly improved heat dissipation, which was consistent with the estimation results. Furthermore, thermal resistance measurements of a simulated module demonstrated that the module using the LSC joint achieved a 13% reduction in thermal resistance compared with that using a conventional solder joint. The findings of this study provide clear design guidelines for LSC joints and demonstrate their strong potential for advancing the thermal management of next-generation, high-power-density electronic devices.

1. Introduction

Recently, the demand for power electronics has increased across various fields, including electric vehicles and renewable energy applications, where cost reduction and high efficiency are required [1,2]. Therefore, power modules, which are key components of power electronics, must become smaller, lighter, and more efficient. To meet these demands, wide-bandgap (WBG) semiconductor materials, such as silicon carbide and gallium nitride, have been used as alternatives to conventional Si devices [3–6]. WBG semiconductor materials enable high-temperature operations and device miniaturization. However, higher operating temperatures and increased power densities can lead to thermal degradation and fatigue failure, particularly in bonding layers such as die-attached and base-attached layers. Therefore, it is essential to improve heat dissipation in the bonding layer.

Bonding technologies commonly used in power modules include soldering, Ag sintering, and transient liquid phase (TLP) bonding. Among these, soldering is widely used owing to its simplicity and low cost. However, solder materials generally exhibit low thermal conductivities, resulting in poor heat dissipation. Ag sintering provides excellent thermal conductivity and high heat resistance but involves a complex process [7]. TLP bonding is as simple as conventional soldering; however, it suffers from low thermal conductivity and requires long bonding times [8]. Therefore, developing a bonding technology that combines a simple process with high heat dissipation performance is crucial.

To improve the joint performance, new bonding technologies that combine Cu and Sn-based solders have been reported. Zhang et al. [9] fabricated a Cu@Sn core–shell composite powder and its bonded structure, demonstrating excellent mechanical, thermal, and electrical properties. Xu et al. [10] proposed a Cu/solder composite structure fabricated by cross-accumulative rolling technique using Cu powder and

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https://doi.org/10.1016/j.jmrt.2026.02.028
Received 28 November 2025; Received in revised form 30 January 2026; Accepted 2 February 2026
Available online 5 February 2026

Sn foil. Heo et al. [11] proposed a new Cu/Sn composite structure using Cu foam and Cu–Sn paste, which exhibited high thermal reliability and superior mechanical properties. Zhu et al. [12] compared joints fabricated using pure Sn, Sn/Cu powder composite solder, and Sn/Cu foam composite solder considering the microstructure, electrical resistivity, thermal conductivity, and shear strength. Notably, the Sn/Cu foam composite solder joints exhibited the lowest electrical resistivity, highest thermal conductivity, and greatest shear strength. These studies indicate that combining Cu and solder enables the fabrication of joints with excellent properties and that mixing Cu into solder in various forms can yield diverse performance characteristics. Cu/solder composite structures are highly effective for thermal dissipation. However, their fabrication processes are generally more complicated than those for conventional soldering.

In our previous study [13], we proposed a Cu/solder composite structure using lotus-type porous copper (lotus Cu) with unidirectionally aligned pores and investigated its thermal conductivity and high-temperature reliability. By placing lotus Cu beneath the solder foil and heating it in a reflow oven, the molten solder infiltrated the pores of lotus Cu, resulting in successful bonding. The fabricated anisotropic lotus Cu/solder composite (LSC) structure exhibited excellent thermal conductivity and high-temperature reliability, demonstrating that highly heat-dissipative joints can be fabricated through a simple conventional soldering process [14]. Moreover, a similar approach using lotus Cu has been reported to be applicable to soldering or TLP bonding [15,16]. However, the relationship between the microstructure of the LSC and its heat dissipation performance has not yet been thoroughly investigated. To further reduce thermal resistance, it is necessary to examine joint structures that provide a lower thermal resistance.

In this study, distinguishing this work from our previous feasibility studies [13,14], the relationship between the microstructure and thermal resistance of an LSC joint was systematically investigated, and its practical applicability was demonstrated using a simulated power module. Initially, the structural parameters affecting heat dissipation were estimated using the rule of mixtures. The bonding process was examined to control structural parameters. Subsequently, the equivalent thermal conductivities and thermal resistances of the fabricated LSC joints were measured and compared based on structural differences. Finally, a simulated power module was fabricated, and the thermal resistance of the module with the LSC joint was compared with that of a conventional solder joint. Based on these results, design guidelines for achieving low thermal resistance in LSC joints were proposed.

2. Method

2.1. Sample preparation

The LSC joint was fabricated using a lotus Cu sheet, solder sheet, and Cu substrate. Lotus Cu sheets were provided by Lotus Thermal Solution, Inc. (Japan) with a thickness of 0.2 mm and average porosity of 56%. The specimens were cut into disks with diameters of 10 mm, as shown in Fig. 1(a). Commercial Sn–3Ag-0.5Cu (SAC305) sheets with thicknesses of 0.10, 0.12, 0.15 mm (Nihon Handa Co., Ltd., Japan) were used as solder sheets. The solder sheets were then cut into disks with a diameter

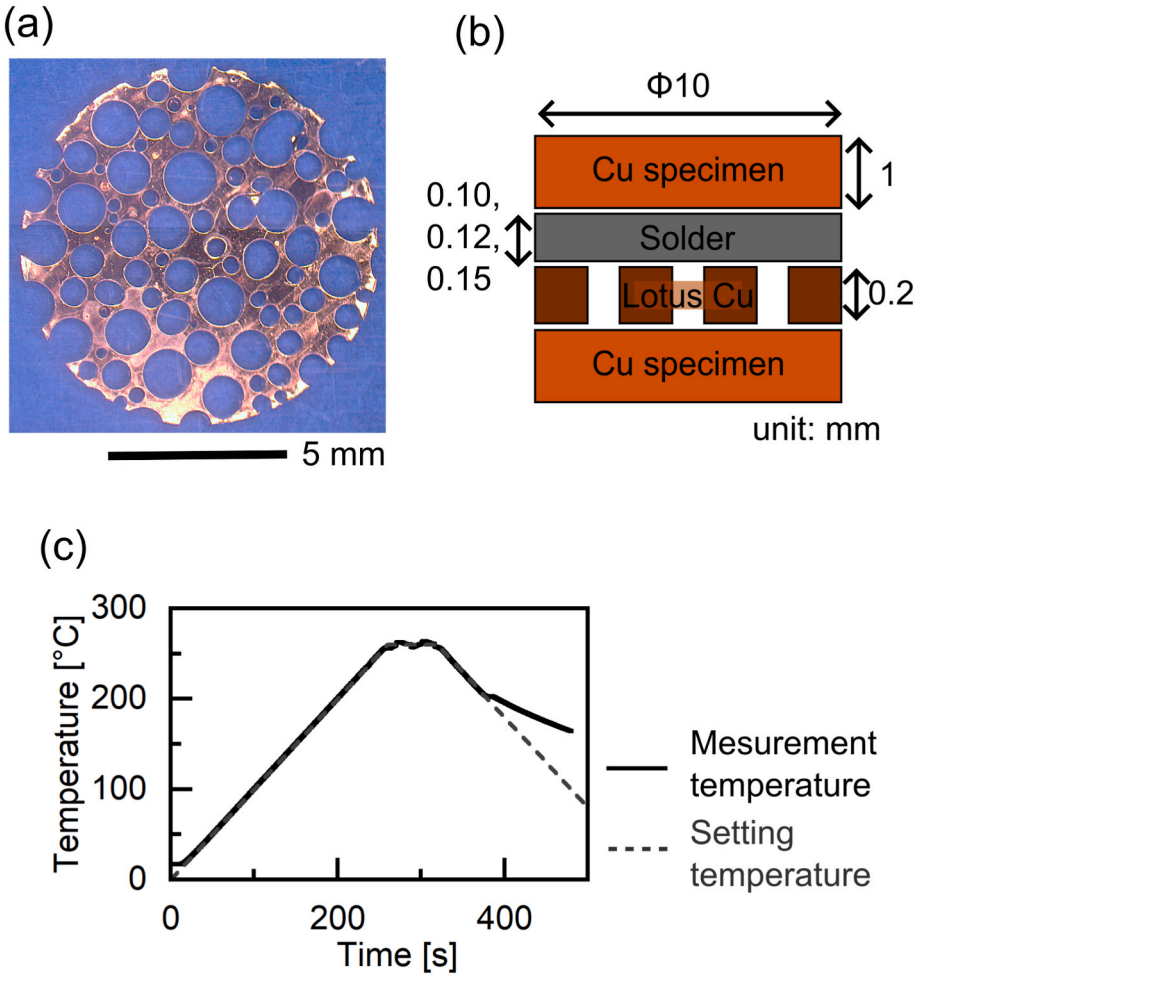

Fig. 1. Bonding process of Cu/solder composite joint structure. (a) Lotus-type porous Cu cut into 10 mm diameter pieces. (b) Schematic of sample. (c) Temperature profile during bonding.

of 10 mm. The Cu specimen was a disk with a diameter of 10 mm and a thickness of 1 mm. The pore area of the lotus Cu was analyzed using ImageJ software. In this study, the solder/pore volume ratio was used to evaluate the amount of solder. The solder/pore volume ratio was calculated as the ratio of the solder sheet volume to the lotus Cu pore volume.

Before bonding, we sequentially cleaned the lotus Cu, solder sheet, and Cu disk with 4% HCl, distilled water, and ethanol. We then dipped them in flux (SR-12, Senju Metal Industry Co., Ltd., Japan) and stacked them, as shown in Fig. 1(b). The temperature profile during bonding is shown in Fig. 1 (c). Subsequently, we heated the samples at 260 °C for 1 min under pressures of 0, 2.03, 6.48, and 10.4 kPa in a reflow oven (SK-5000; Sanyoseiko Co., Ltd., Japan). We then prepared the samples by conventional reflow without pressure reduction during heating and vacuum reflow with two pressure reductions.

2.2. Characterizations

In this study, the microstructures of the joints, particularly the solder thickness and void fraction, and their thermal properties were evaluated. The thicknesses of the lotus Cu and Cu specimens before bonding and that of the bonded samples were measured using a micrometer. In this study, the solder thickness was defined as the bonded sample thickness minus the prebonding thicknesses of the lotus Cu and Cu specimens. Voids in the joints were observed using scanning acoustic tomography (SAT, Fine SAT, Hitachi Power Solutions Co., Ltd., Japan), and the void fraction was analyzed using ImageJ software. Cross-sections of the joints, prepared by grinding with SiC grit papers followed by polishing with colloidal silica suspension, were observed using a scanning electron microscope (JSM-IT200, JEOL Ltd., Japan). The equivalent thermal conductivity and thermal resistance of the LSC joints were evaluated using a steady-state method. Fig. 2(a) shows a schematic of the sample prepared for the experiment. For accurate measurements, the bonding layer was stacked into five layers. The upper and lower Cu specimens were disks with a diameter of 10 mm and a thickness of 3 mm, each having a hole with a diameter of 1 mm and a depth of 1.5 mm from the surface. Fig. 2(b) shows a schematic of the measurement setup (TCM1001; Rhesca Co., Ltd., Japan). Cu rods were placed above and below the sample, and a heater and cooler were placed at the top and bottom, respectively. Each Cu rod contained five holes, spaced 5 mm apart. The heater and cooler were maintained at 200 and 5 °C, respectively. To prevent heat loss, grease was applied between the materials, as shown in Fig. 2(b), and the Cu rods and samples were covered with glass wool. After reaching the steady-state condition, the temperatures at the 12 points, as shown in Fig. 2(b), were measured using thermocouples. Fig. 2(c) presents an example of the relationship between the measured temperature and the distance between the measurement points.

The equivalent thermal conductivity and thermal resistance of the LSC joints were calculated following the procedure outlined in our previous study [13]. The temperature slopes of the distances (dT/dx) for each rod were obtained by linear fitting. The amount of heat Q is then obtained using Fourier's law as follows:

$$Q = \lambda_{Cu} \cdot A \cdot \frac{dT}{dx}, \tag{1}$$

where λ_{Cu} is the thermal conductivity of Cu and A is the heat flow area. Using the calculated Q and Fourier's law, the thermal resistance of the joint R_{bond} is calculated using Q and Fourier's law as follows:

$$R_{bond} = \frac{\Delta T_{bond}}{Q}, \tag{2}$$

where ΔT_{bond} is the temperature difference of the joint. The equivalent thermal conductivity of the joint, λ_{bond}, is obtained as follows:

$$\lambda_{bond} = \frac{t_{bond}}{R_{bond} \cdot A}. \tag{3}$$

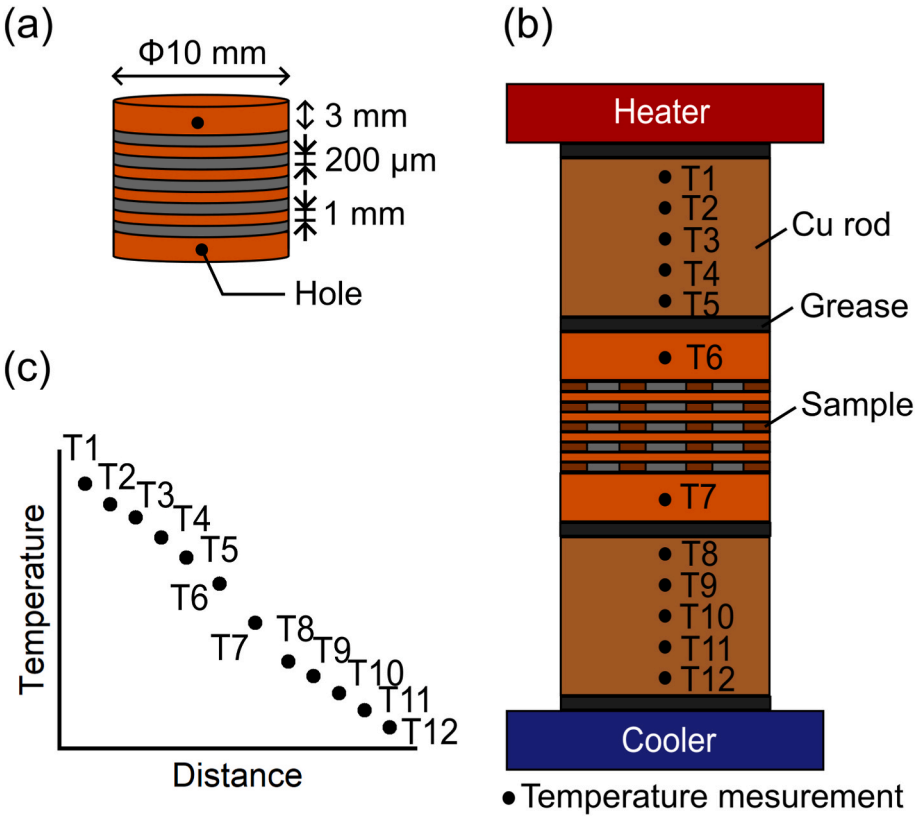

Fig. 2. Steady-state thermal conductivity measurement. Illustration of (a) sample, (b) measurement setup, and (c) measured temperature data.

Nine measurements were conducted for each sample, and the average values were used to determine the equivalent thermal conductivity and thermal resistance.

2.3. Thermal characteristic test with module

To evaluate the heat transfer performance of the LSC joint in practical applications, a single-sided cooling (SSC) power module is fabricated, as shown in Fig. 3. A schematic of the cross-sectional structure is shown in Fig. 3(a). The module consisted of a test element group (TEG) chip with a built-in resistance heater circuit, an insulated circuit substrate, and a heat spreader, which were bonded by die-attached and base-attached layers. The TEG chip was a Si chip with dimensions of 5 mm × 5 mm × 0.4 mm. The insulated circuit substrate had a cross-sectional structure of Cu/Si_3N_4/Cu with layer thicknesses of 0.3, 0.32, and 0.3 mm, and an outer dimension of 28 mm × 28 mm (FJ Composite Materials Co., Ltd., Japan), as detailed in our previous work [17]. A schematic of the top-view of the chip and substrate is shown in Fig. 3(b). The chip was die-attached at the center of the substrate. Au wires were used to electrically connect the chip surface to external electrodes. This configuration enabled the heater circuit on the TEG chip to generate heat with a relatively small current, simulating the rise in the chip surface temperature (T_j) of actual power modules. The insulated circuit substrate was attached to a Cu heat spreader (80 mm × 80 mm × 4.5 mm). Two types of modules were prepared for comparison: One using the proposed LSC joint for the die-attached and base-attached layers (LSC module), and another using a conventional solder joint for comparison (conventional solder module). For the LSC module, SAC305 solder sheets with a thickness of 200 μm were used for the die-attached and base-attached layers, corresponding to a solder/pore volume ratio of approximately 1.43, as determined from the findings in Section 3.2. For the conventional solder module, a 100 μm thick solder sheet was used for the die-attached layer, and a 330 μm thick sheet for the base-attached layer to achieve a final thickness of 300 μm. This thickness was selected based on common design practices in industrial applications for high thermomechanical reliability [18]. Bonding for both module types was performed in a formic acid atmosphere at a peak temperature of 260 °C. A vacuum process was applied while the solder was molten to minimize voids, which was consistent with the findings in Section 3.2. To ensure proper bonding, a weight of approximately 11 g was applied on the chip during die attachment, and a weight of 80 g was applied to the substrate during base attachment, corresponding to bonding pressures of 4.3 and 1.2 kPa, respectively. The fabricated SSC power module is mounted on a water cooler using a thermal pad, as shown in Fig. 3(c).

The thermal resistance $R_{th(jc)}$, between the chip surface temperature (T_j) and the temperature at the center of the bottom surface of the heat spreader (T_c) was measured. T_j and T_c were measured immediately after power was applied to the TEG chip heater for 5 s to generate 70 W of heat. $R_{th(jc)}$ is obtained using the following equation:

$$R_{th(jc)} = \left(T_j - T_c\right) / P, \tag{4}$$

where P denotes the heating power. T_c was measured using a thermocouple. T_j was estimated based on the precalibrated temperature dependence of the electrical resistance of the TEG chip heater using a temperature-sensitive electrical parameter-based method [19]. The temperature of the water flowing into the water cooler was maintained at 25 °C. During measurements, the surface temperature of the power module was simultaneously monitored using a thermal imaging camera (InfReC R450, Nippon Avionics Co., Ltd., Japan). To improve the accuracy of the temperature measurements, the surface was coated with a black spray of known emissivity. The entire evaluation sequence was repeated 10 times, and the resulting values were averaged to determine the final $R_{th(jc)}$.

3. Results and discussion

3.1. Estimation

The equivalent thermal conductivity and thermal resistance of the joint were estimated to investigate the microstructural parameters affecting its heat dissipation. In general, the thermal resistance of a composite structure can be calculated using the rule of mixtures [20]. Fig. 4(a) shows the joint obtained from a previous study. Fig. 4(b) and (c) show schematic of the joint corresponding to that shown in Fig. 4(a).

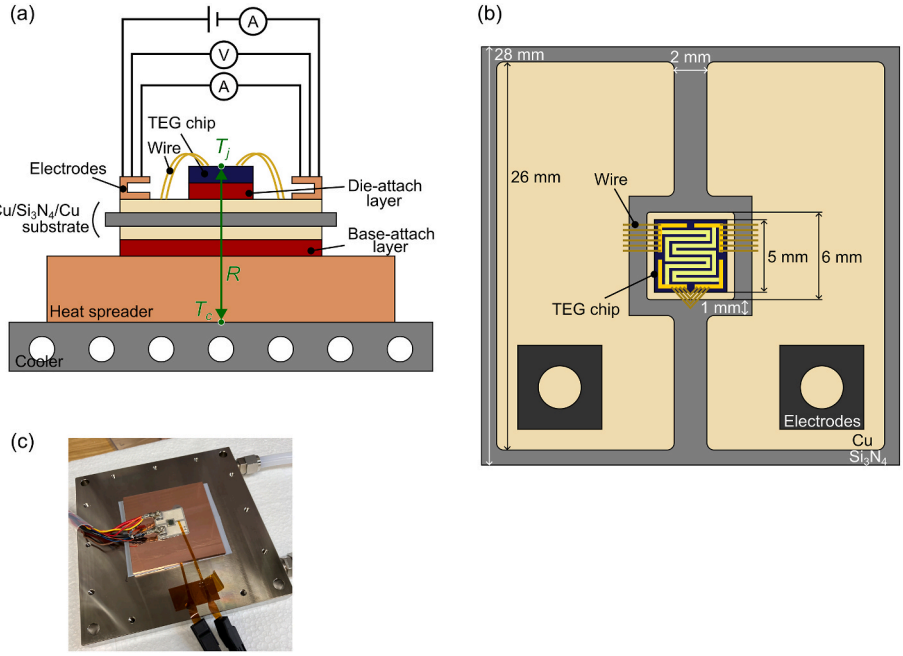

Fig. 3. Thermal characteristic test of single-side cooling (SSC) power module. (a) Schematic of cross-sectional of module structure, indicating measurement points for chip surface temperature (T_j) and heat spreader bottom temperature (T_c). (b) Top view of test element group chip die-attached on insulated circuit substrate. (c) Experimental setup for thermal resistance measurement.

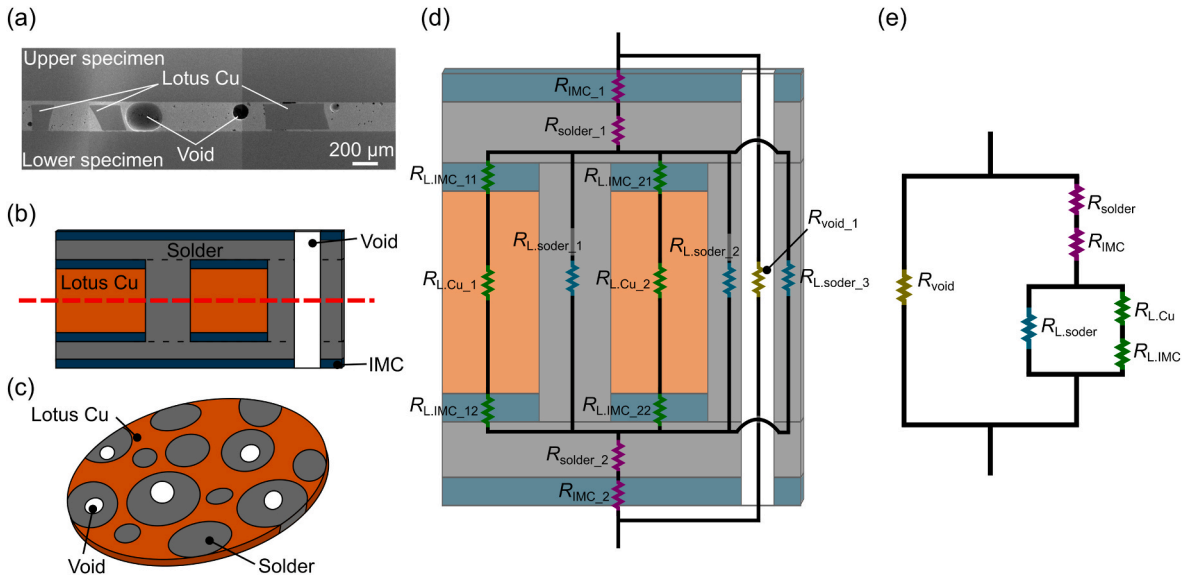

Fig. 4. (a) Cross-sectional scanning electron microscopy (SEM) image of Cu/solder composite joint structure [13]. Schematic of (b) cross section of bonding layer and (c) top view. (d) Thermal network corresponding to (b). (e) Simplified thermal network of (d).

As shown in Fig. 4(a) and (b), the joint has a three-layer structure consisting of an upper solder layer/lotus Cu layer and a solder layer/-lower solder layer. Intermetallic compounds (IMCs) were formed at the lotus Cu/solder and Cu specimen/solder interfaces. The IMC formed on the side surface of the lotus Cu was parallel to the heat flow direction and had only a minimal effect on thermal resistance; therefore, it was not considered in this study. Fig. 4(c) shows a top view of the joint, indicated by the dashed red line, as previously shown in Fig. 4(b). As shown in Fig. 4(c), the pores of lotus Cu are filled with solder, resulting in the formation of voids in some regions.

Fig. 4(d) illustrates a thermal resistance circuit diagram, as previously shown in Fig. 4(b). R_{void_i}, R_{IMC_i}, $R_{L.IMC\_i}$, $R_{L.Cu\_i}$, R_{solder_i}, and $R_{L.solder\_i}$ represent the thermal resistances of the voids, IMC at the Cu specimen/solder interface, IMC at the lotus Cu/solder interface, lotus

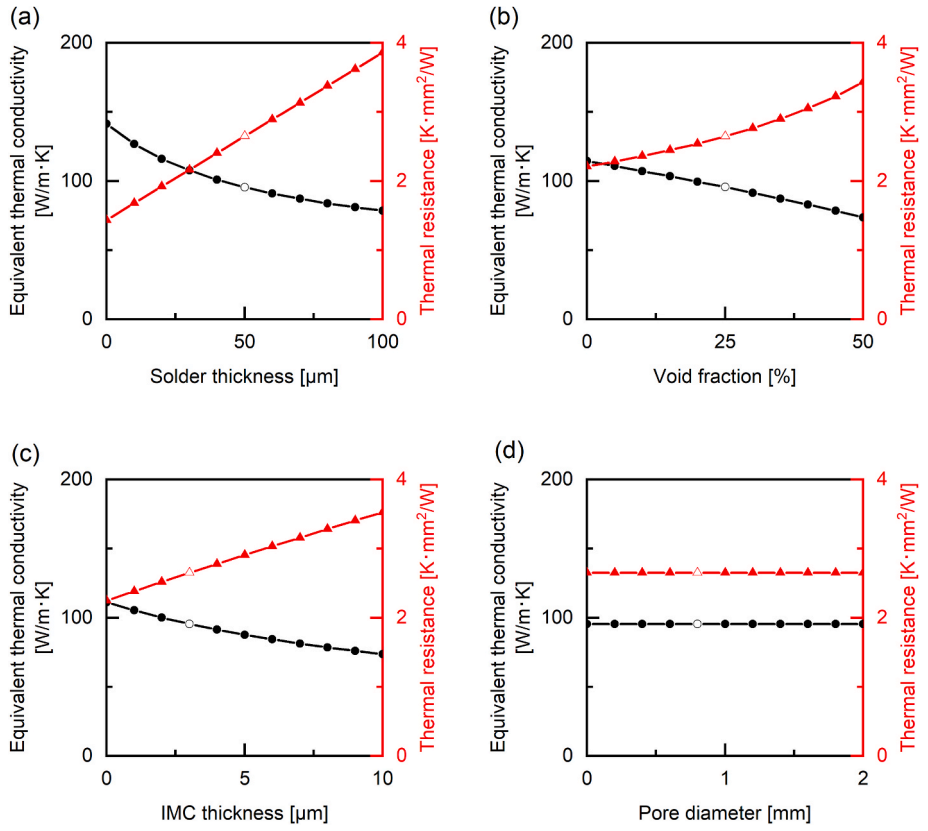

Fig. 5. Estimation results of equivalent thermal conductivity and thermal resistance at different (a) solder thickness with 25% void fraction, 3 μm IMC thickness, and 0.8 mm pore diameter, (b) void fraction with 50 μm solder thickness, 3 μm IMC thickness, and 0.8 mm pore diameter, (c) IMC thickness with 50 μm solder thickness, 25% void fraction, and 0.8 mm pore diameter, and (d) pore diameter with 50 μm solder thickness, 25% void fraction, and 3 μm IMC thickness.

Cu, solder between the lotus Cu and Cu specimen, and solder inside the pores of lotus Cu, respectively. This circuit diagram can be simplified, as shown in Fig. 4(e).

Fig. 5 shows the estimated results for the equivalent thermal conductivity and thermal resistance. The thermal conductivities of materials used in this study are listed in Table 1. SAC305 was used as the standard solder in this study because the influence of differences in solder composition was considered minor compared to the highly thermally conductive Cu (400 W/m·K). The thickness and porosity of lotus Cu were 200 μm and 56%, respectively. Based on the standard conditions obtained in a feasibility study (solder thickness 50 μm, void fraction 25%, IMC thickness 3 μm, and pore diameter 0.76 mm), the equivalent thermal conductivity and thermal resistance were estimated while varying the solder thickness, void fraction, IMC thickness, and pore diameter. It should be noted that the interfacial thermal resistance was not explicitly considered. As this estimation serves as a first-order approximation to identify dominant structural factors, the analysis focused on bulk thermal resistance, assuming interfacial contribution to be minor at this scale. Fig. 5(a) shows the relationship between solder thickness, equivalent thermal conductivity, and thermal resistance. When the solder thickness decreases from 50 to 0 μm, the equivalent thermal conductivity increases from 96 to 141 W/m·K (+48%), while the thermal resistance decreases from 2.65 to 1.44 K mm^2/W (−46%), as shown in Fig. 5(a). Fig. 5(b) shows the relationship between the void fraction, equivalent thermal conductivity, and thermal resistance. The results in Fig. 5(b) indicate that when the void fraction decreases from 25% to 0%, the equivalent thermal conductivity increases from 96 to 115 W/m·K (+20%), while the thermal resistance decreases from 2.65 to 2.21 K mm^2/W (−17%). Fig. 5(c) shows the relationship between the IMC thickness, equivalent thermal conductivity, and thermal resistance. The results in Fig. 5(c) indicate that when the IMC thickness decreases from 3 to 0 μm, the equivalent thermal conductivity increases from 96 to 111 W/m·K (+16%), while the thermal resistance decreases from 2.65 to 2.25 K mm^2/W (−15%). Fig. 5(d) shows the relationship between pore diameter, equivalent thermal conductivity, and thermal resistance. The results in Fig. 5(d) indicate that the pore diameter has no significant effect on the equivalent thermal conductivity and thermal resistance. These results demonstrated that reducing the solder thickness, void fraction, and IMC thickness effectively improved heat dissipation performance of the LSC joint. Among these factors, IMC thickness is strongly affected by the sample structure and bonding temperature, making precise control difficult. Therefore, in this study, the effects of the solder thickness and void fraction on the equivalent thermal conductivity and thermal resistance were experimentally investigated.

3.2. Bonding process

Fig. 6 shows the cross-sections of the LSC joint. These results confirmed successful bonding between the lotus Cu and solder. Fig. 6(a) and (d) show the cross-section at a solder/pore volume ratio of 1.23, where few voids and thin solder layers at the top and bottom are observed. At a ratio of 0.88 (Fig. 6(b–e)), the solder layer is thin and contains numerous voids. In contrast, at a ratio of 1.66 (Fig. 6(c–f)), a few voids but thick solder layers are observed. These results indicate that the joint structure can be controlled by varying the joining conditions.

To control the solder thickness and void fraction, the effects of the vacuum processing, bonding pressure, and solder/pore volume ratio on these parameters were investigated. Fig. 7(a) shows a comparison of conventional and vacuum reflows. The solder volume fraction was 1.23, and the bonding pressure was 0 kPa. Under vacuum reflow, compared with conventional reflow, the solder thickness decreased from 173 to 22 μm (−87%), and the void fraction decreased from 25.5% to 2.3% (−91%). These results indicate that vacuum reflow is effective in promoting the infiltration of molten solder into the pores of lotus Cu, leading to the reduction of solder thickness and void fraction.

Fig. 7(b) shows the effect of the solder/pore volume ratio on the solder thickness and void fraction. Vacuum reflow was used and the bonding pressure was 0 kPa. As the solder/pore volume ratio increased from 0.62 to 1.64, the solder thickness increased from 0 to 68 μm, while the void fraction decreased from 27.8% to 1.4%. When the solder/pore volume ratio was less than 1, the pore volume was larger than the solder volume; therefore, not all pores can be filled with solder, resulting in a high void fraction. Additionally, because the solder preferentially infiltrated the pores, the solder thickness decreased. When the solder/pore volume ratio was less than 1, the solder volume exceeded the pore volume, and all the pores were filled with solder, resulting in a low void fraction. In contrast, excess solder overflowed from the pores and remained above and below the lotus Cu, leading to an increased solder thickness.

Fig. 7(c) shows the effect of the bonding pressure on the solder thickness and void fraction. Vacuum reflow was used and the solder/pore volume ratio was 1.28. Within the pressure range of 0–10.4 kPa, the solder thickness was approximately 25 μm, and no significant correlation between pressure and solder thickness was observed. Without applied pressure, the void fraction was 2.3%, and when the bonding pressure exceeded 2.03 kPa, the void fraction increased slightly with increasing pressure. This slight increase in void fraction at higher pressures is attributed to the restriction of gas escape pathways for expanding bubbles during the vacuum reflow process. The effect of pressure was found to be limited.

3.3. Thermal properties

The equivalent thermal conductivity and thermal resistance of LSC joints with different structures were measured to clarify the relationship between the solder thickness, void fraction, and thermal properties. Fig. 8 shows the effects of solder thickness and void fraction on equivalent thermal conductivity and thermal resistance. A color map was generated by triangulation and linear interpolation based on the measured points. At a solder thickness of 16 μm and a void fraction of 3%, the equivalent thermal conductivity reached 100 W/m·K and the thermal resistance was minimized at 2.15 K mm^2/W. For a solder joint with comparable thickness and void fraction, the thermal resistance was estimated to be 4.05 K mm^2/W, demonstrating a 47% reduction when using lotus Cu. Additionally, with decreasing solder thickness and void fraction, the equivalent thermal conductivity increased, and the thermal resistance decreased. This tendency is in agreement with the estimated results shown in Fig. 5. Although some discrepancies exist between the experiment and estimation, estimation using the rule of mixtures is effective for understanding structural effects on thermal properties.

Furthermore, the thermal performance of the LSC joint was compared with that of recently reported bonding technologies utilizing Cu fillers or porous Cu. Regarding transient liquid phase sintering (TLPS) using Cu fillers, Greve et al. [23] reported equivalent thermal conductivities ranging from 95.7 to 189.0 W/m·K for Cu–Sn TLPS joints. However, these values were achieved under relatively severe processing conditions of 300 °C for 30 min with an applied pressure of 300 kPa. As for methods utilizing porous Cu, Wang et al. [24] and Zhu et al. [12] fabricated composite joints by infiltrating solder into Cu foam. While the large specific surface area of the Cu foam promotes isothermal solidification for high-temperature resistance, the resulting thermal conductivity was limited to approximately 58.9–68.3 W/m·K. This limitation is attributed to the disordered morphology of Cu foam and the extensive formation of IMCs, which disrupt the thermal pathways via Cu. In

Table 1
Thermal conductivity of materials for estimation [21,22].

Material	Thermal conductivity [W/m·K]
Sn	55
Cu	400
IMC (Cu_6Sn_5)	34.1

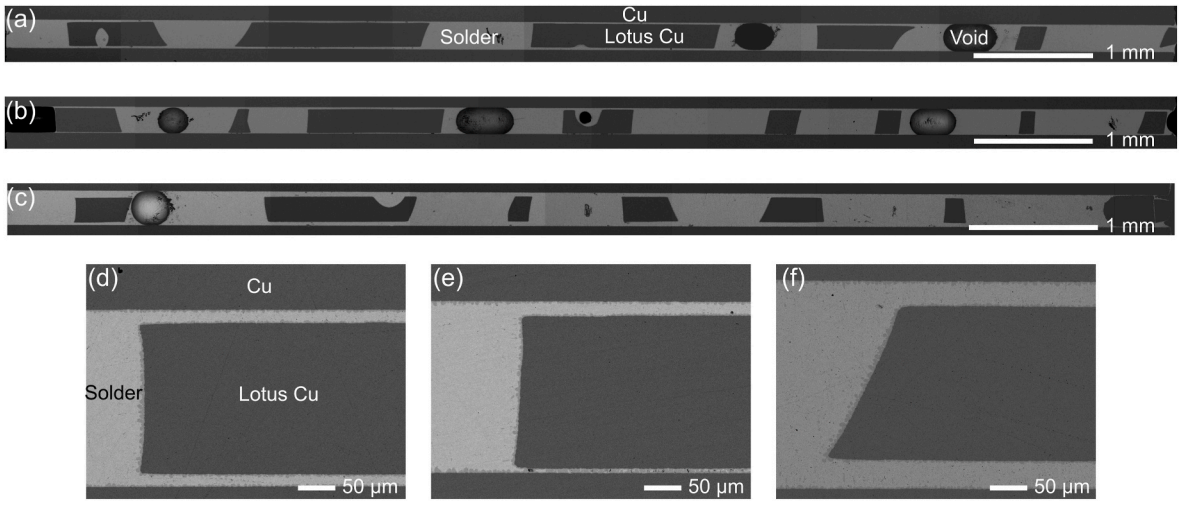

Fig. 6. Cross-sectional SEM images of lotus Cu/solder composite structure (LSC) joint with solder/pore volume ratios of (a) 1.23, (b) 0.88, and (c) 1.66. (d–f) Magnified views of (a–c), respectively.

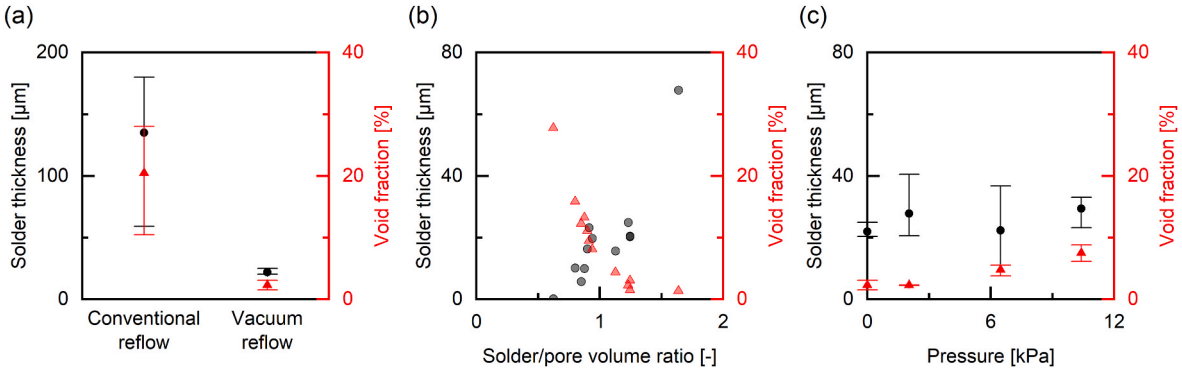

Fig. 7. (a) Solder thickness and void fraction in conventional and vacuum reflows. Solder thickness and void fraction with different (b) solder/pore volume ratio and (c) pressure in vacuum reflow. In (a) and (c), the data points represent the average values, and the error bars indicate the range between the maximum and minimum values. The data in (b) are plotted as raw values.

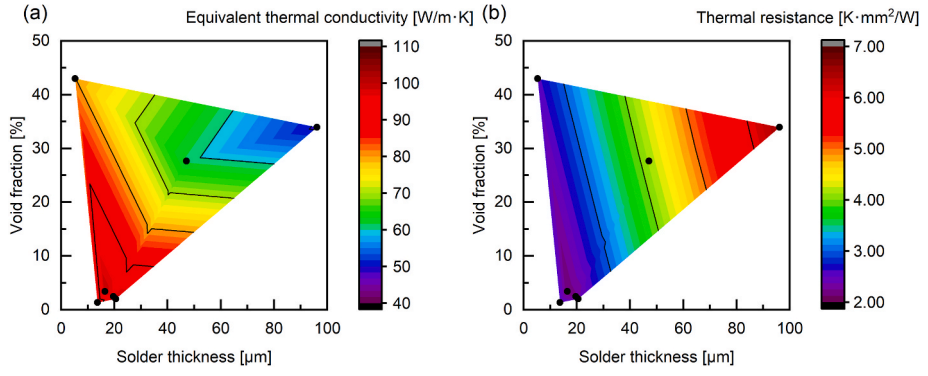

Fig. 8. Experimental (a) equivalent thermal conductivity and (b) thermal resistance results.

contrast, the LSC joint in this study achieved a high equivalent thermal conductivity of approximately 100 W/m·K through a rapid and simple conventional reflow process. This high performance stems from the unique structure of the lotus Cu, where the pores are unidirectionally aligned parallel to the heat dissipation direction. This alignment ensures that the thick, continuous Cu pillars function as an effective thermal path, thereby bypassing the high thermal resistance of the solder and IMC layers. Moreover, our previous study demonstrated that decreasing the porosity of lotus Cu to 51% (i.e., increasing the Cu volume fraction) resulted in a maximum thermal conductivity of 142.4 W/m·K [13]. These comparisons indicate that the LSC joint offers a superior balance of high thermal performance and manufacturing efficiency, with the potential for further improvement by controlling the porosity.

3.4. Thermal characteristics of the SSC power module

The heat dissipation characteristics of the fabricated SSC power modules were evaluated to demonstrate the effectiveness of the LSC

joint. The thermal performance of the LSC module was compared with that of a conventional solder module. The results are shown in Fig. 9. The X-ray transmission observation of the conventional solder module, as shown in Fig. 9(a), reveals that the die-attached and base-attached layers are well-formed with some minor voids. Similarly, the observation of the LSC module indicates a sound bonding state, as shown in Fig. 9(b). The final thicknesses of the die-attached and base-attached layers in the conventional solder module were 93.2 and 308 μm, respectively. In the LSC module, the total joint thicknesses of the die-attached and base-attached layers were 243.5 and 286.6 μm, respectively. These joints consisted of a 200 μm thick lotus-Cu core, resulting in residual solder thicknesses of 43.5 and 86.6 μm.

The thermal resistance $R_{th(jc)}$ is determined, as shown in Fig. 9(c). The $R_{th(jc)}$ for the module with conventional solder joints was 1.09 K/W, whereas the module with LSC joint exhibited a lower value of 0.94 K/W. This result indicated that the LSC joint reduced the thermal resistance by approximately 13%, even when using a simple reflow process. Notably, this reduction was achieved even though the total combined thickness of the die-attached and base-attached layers in the LSC module (approx. 530 μm) was significantly greater than that of the conventional solder module (approx. 401 μm). Fig. 9(d) and (e) show the surface temperature distributions of the SSC power modules immediately after applying 70 W of heat for 5 s in the solder and LSC cases, respectively. The corresponding temperature profiles at the center of the chip surface are shown in Fig. 9(f). The maximum chip surface temperatures were 116 and 102 °C for the solder and LSC cases, respectively. This finding demonstrated that the chip surface temperature in the LSC module was approximately 14 °C lower than in the solder module. Furthermore, the thermal images (Fig. 9(d) and (e)) confirm that the surface temperature of the surrounding insulated circuit substrate is correspondingly lower in the LSC case. These results clearly demonstrate the superior heat dissipation capability of the LSC joint in practical module applications.

4. Conclusion

An LSC joint with low thermal resistance was fabricated, and the relationship between the joint structure and thermal properties was investigated. The following conclusions were drawn.

1. The LSC joint was fabricated by infiltrating molten solder into the pores of lotus Cu. To obtain high-quality joints with thin solder layers and low void fractions, vacuum reflow, an appropriate solder volume comparable to the pore volume, and low bonding pressure are important.
2. The thermal properties of LSC joints were measured using the steady-state method. When the solder thickness was 16 μm and the void fraction was 3%, the thermal resistance reached a minimum of 2.15 K mm^2/W, while the equivalent thermal conductivity reached a maximum of 100 W/m·K. Notably, reducing the solder thickness and

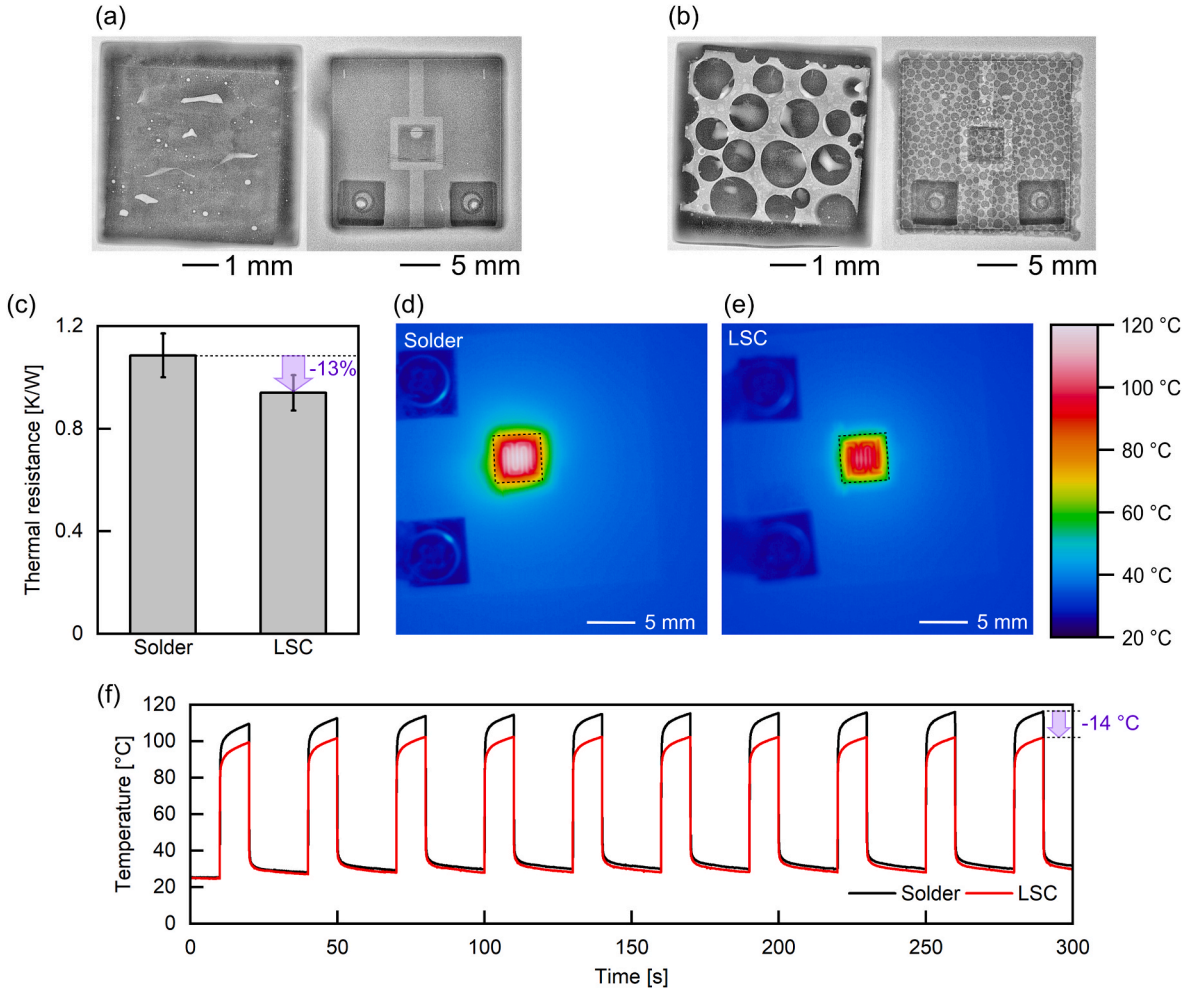

Fig. 9. Thermal characteristics of SSC power module. X-ray transmission images of die-attached and base-attached layers with (a) conventional solder module and (b) LSC module. (c) Comparison of thermal resistance ($R_{th(jc)}$) between conventional solder and LSC modules. Surface temperature distributions of (d) conventional solder module and (e) LSC module immediately after a 5 s, 70 W heat input. (f) Temperature transients at center of chip surface during cyclic heating.

void fraction was effective for improving heat dissipation, which was consistent with the estimation based on the rule of mixtures.

3. The practical heat dissipation performance of the LSC joint was demonstrated using an SSC power module. The module utilizing the LSC joint achieved a 13% reduction in thermal resistance compared with that using conventional solder joints, highlighting its superior heat dissipation capability in practical applications.

These findings provide clear design guidelines for LSC joints and demonstrate their strong potential for advancing the thermal management of next-generation, high-power-density electronic devices. Further evaluating the reliability of LSC joints under harsh environments, such as severe cyclic temperature changes, high vibration, and humidity, is of particular interest.

Data statement

Data will be made available on request.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This study was partly supported by the Project on Design & Engineering by Joint Inverse Innovation for Materials Architecture (DEJI^{2}MA) under the Ministry of Education, Culture, Sports, Science, and Technology (MEXT), Japan.

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